CLAIMS

We claim:

1. An apparatus for defining a computer readable definition of a photolithographic mask of a target pattern in a layer of material of an integrated circuit, the target pattern comprised of a plurality of features, the apparatus comprising:

means for defining a maximum shifter area around the plurality of features in the target pattern;

means for placing shifter shapes in the computer readable definition of the photolithographic mask, the shifter shapes placed within the maximum shifter area such that the shifter shapes run along edges of the plurality of features and such that space is left between adjacent shifter shapes to admit a cut;

means for assigning phase to the plurality of shifter shapes according to phase dependencies and costs;

means for refining the shifter shapes; and

means for outputting the computer readable definition of the photolithographic mask including the plurality of shifter shapes.

2. The apparatus of claim 1, further comprising means for producing a computer readable definition of a complementary photolithographic mask from the target pattern and the plurality of shifter shapes.

3. The apparatus of claim 1, wherein the means for assigning further comprises means for computing a cost for a given phase assignment to a phase shifter in the plurality of shifter shapes, the cost corresponding to the relative quality of the given phase assignment.

4. An article of manufacture comprising a computer readable storage medium, having stored thereon computer readable instructions for definition of a photolithographic mask that define a target pattern in a layer to be formed using the mask, wherein said pattern includes a plurality of features; the computer readable instructions comprising:

a first set of instructions for accessing the target pattern;

a second set of instructions for defining a maximum shifter area around the plurality of features in the target pattern;

a third set of instructions for placing shifter shapes in the computer readable definition of the photolithographic mask, the shifter shapes placed within the maximum shifter area such that the shifter shapes run along edges of the plurality of features and such that space is left between adjacent shifter shapes to admit a cut;

a fourth set of instructions for assigning phase to the plurality of shifter shapes according to phase dependencies and costs;

a fifth set of instructions for refining the shifter shapes; and

a sixth set of instruction for storing the computer readable definition of the photolithographic mask.

5. The article of manufacture of claim 4, wherein the fourth set of instructions further comprises a set of instructions for using a plurality of cost functions to describe the relative quality of accepting a particular phase assignment, the plurality of cost functions including one or more of an inner corner cost function, an outer corner cost function, a three edge cost function, a small shifter area cost function, a phase conflict cost function, and a multi-layer cost function.

6. The article of manufacture of claim 4, wherein the fourth set of instructions further comprises a set of instructions for performing branch-and-bound to assign phase.

7. The article of manufacture of claim 4, wherein the second set of instructions further comprises a set of instructions for growing a boundary around the plurality of features except at end-caps to define the maximum shifter area.

8. The article of manufacture of claim 4, wherein the second set of instructions further comprises a set of instructions for defining a minimum shifter area and an endcap cutting protection, and where the defining the maximum shifter area accounts for the endcap cutting protection.

9. The article of manufacture of claim 4, wherein the second set of instructions further comprises a set of instructions for clustering the plurality of features into a plurality of groups, each group susceptible to independent parallel processing through the third, fourth, and fifth set of instructions.

10. The article of manufacture of claim 9, wherein the second set of instructions further comprises a set of instructions for defining a minimum shifter area and an endcap cutting protection, and where the defining the maximum shifter area protects the endcap cutting protection.

11. A photolithographic mask of a target pattern in a layer of material of an integrated circuit, the target pattern comprised of a plurality of features, the photolithographic mask comprising:

a plurality of shifter shapes within a maximum shifter area around the plurality of features in the target pattern, such that the shifter shapes run along edges of the plurality of features, the plurality of shifter shapes having phases assigned according to phase dependencies and costs, the plurality of shifter shapes having one or more refinements filling at least part of space originally left between adjacent shifter shapes to admit a cut.

12. The mask of claim 11, further comprising a complementary photolithographic mask from the target pattern and the plurality of shifter shapes.

13. The mask of claim 11, wherein the phases are computed according to costs corresponding to a plurality of cost functions to describe the relative quality of accepting a particular phase assignment, the plurality of cost functions including one or more of an inner corner cost function, an outer corner cost function, a three edge cost function, a small shifter area cost function, a phase conflict cost function, and a multi-layer cost function.

14. The mask of claim 11, wherein the phases are assigned via branch-and-bound.

15. The mask of claim 11, wherein the maximum shifter area includes one or more end-caps of at least one feature of the plurality of features.

16. The mask of claim 11, wherein the maximum shifter area accounts for endcap cutting protection.

17. The mask of claim 11, wherein the maximum shifter area is defined by spatially padding the plurality of features with a distance and drawing a border around the plurality of features so that the border is spaced away from the plurality of features by the distance.

18. The mask of claim 17, wherein the border of the maximum shifter area runs closer than the distance to features of the plurality of features having at least one endcap.

19. An integrated circuit produced from a photolithographic mask of a target pattern in a layer of material of the integrated circuit, the layer of material of the integrated circuit comprising:

a plurality of features defined by a plurality of shifter shapes of the photolithographic mask within a maximum shifter area around the plurality of features in the target pattern, such that the shifter shapes run along edges of the plurality of features, the plurality of shifter shapes having phases assigned according to phase dependencies and costs, the plurality of shifter shapes having one or more refinements filling at least part of space originally left between adjacent shifter shapes to admit a cut.

20. The integrated circuit of claim 19, wherein at least one feature of the plurality of features was defined by a complementary photolithographic mask from the target pattern and the plurality of shifter shapes.

21. The integrated circuit of claim 19, wherein the phases are computed according to costs corresponding to a plurality of cost functions to describe the relative quality of accepting a particular phase assignment, the plurality of cost functions including one or more of an inner corner cost function, an outer corner cost function, a three edge cost function, a small shifter area cost function, a phase conflict cost function, and a multi-layer cost function.

22. The integrated circuit of claim 19, wherein the phases are assigned via branch-and-bound.

23. The integrated circuit of claim 19, wherein the maximum shifter area includes one or more end-caps of at least one feature of the plurality of features.

24. The integrated circuit of claim 23, wherein the maximum shifter area accounts for endcap cutting protection.

25. The integrated circuit of claim 19, wherein the maximum shifter area is defined by spatially padding the plurality of features with a distance and drawing a border around the plurality of features so that the border is spaced away from the plurality of features by the distance.

26. The integrated circuit of claim 25, wherein the border of the maximum shifter area runs closer than the distance to features of the plurality of features having at least one endcap.

27. A method of manufacturing an integrated circuit having a layer of material described by a layout, the method comprising:

identifying a plurality of features in the layout to be defined using phase shifting;

exposing radiation sensitive material to radiation according to the target pattern defined using a plurality of shifter shapes of a photolithographic mask within a maximum shifter area around a plurality of features in the target pattern, such that the shifter shapes run along edges of the plurality of features, the plurality of shifter shapes having phases assigned according to phase dependencies and costs, the plurality of shifter shapes having one or more refinements filling at least part of space originally left between adjacent shifter shapes to admit a cut; and

developing the exposed radiation sensitive material to define the layout, and forming said layer of material according to the layout.

28. The method of claim 27, wherein at least one feature of the plurality of features was defined by a complementary photolithographic mask from the layout and the plurality of shifter shapes.

29. The method of claim 27, wherein the phases are computed according to costs corresponding to a plurality of cost functions to describe the relative quality of accepting a particular phase assignment, the plurality of cost functions including one or more of an inner corner cost function, an outer corner cost function, a three edge cost function, a small shifter area cost function, a phase conflict cost function, and a multi-layer cost function.

30. The method of claim 27, wherein the phases are assigned via branch-and-bound.

31. The method of claim 27, wherein the maximum shifter area includes one or more end-caps of at least one feature of the plurality of features.

32. The method of claim 31, wherein the maximum shifter area accounts for endcap cutting protection.

33. The method of claim 27, wherein the maximum shifter area is defined by spatially padding the plurality of features with a distance and drawing a border around the plurality of features so that the border is spaced away from the plurality of features by the distance.

34. The method of claim 33, wherein the border of the maximum shifter area runs closer than the distance to features of the plurality of features having at least one endcap.